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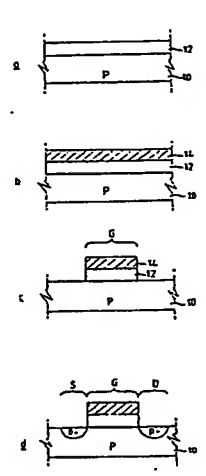
The application is published incomplete as filed (Article 93 (2) EPC). The point in the description or the claim(s) at which the omission obviously occurs has been left blank.
A request for addition of the missing page 9 (parts of claims 3 + 4) has been filed pursuant to Rule 88 EPC. A decision on the request will be taken during the proceedings before the Examining Division (Guidelines for Examination in the EPO, A-V, 2.2).

(54) Manufacturing electronic devices.

(57) The invention provides a process for manufacturing an electronic device on a semiconducting substrate (10) which is transparent to light of a particular wavelength. The process includes the steps of treating the substrate to form at least one region (S,D) having a different electrical property to the substrate, and defining a conducting contact (18) for the regionn by selective photolithographic masking and chemical etching. A layer of photoresist material (16) deposited on one side of the substrate is subjected to light transmitted through the substrate from a light source on the other side of the substrate. The process can be used to produce a field effect transistor on a diamond substrate.



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Description

MANUFACTURING ELECTRONIC DEVICES

This invention relates to a method for manufacturing electronic devices and is particularly applicable to the manufacture of a field effect transistor from diamond material, and to transistors formed by the method.

Field effect transistors (FETs) have been manufactured which comprise a generally conventional FET structure formed on a substrate of diamond, instead of a silicon substrate. The physical properties of diamond result in it having superior characteristics to silicon (Si), gallium arsenide (GaAe) or other known semi-conductive materials in this application. In particular, diamond FETs can be expected to have a lower on resistance, and a higher gain and maximum frequency than transistors employing conventional materials.

Field effect transistors are conventionally formed with the aid of photolithographic masking and chemical etching processes, whereby the source, gate and drain areas of the transistor are demarcated photolithographically, using photo-resist materials, and various mask layers deposited on the substrate of the transistor are selectively removed by etching to define the source, gate and drain regions, as well as metallic contacts for those regions. Due to the small size of the transistor structure, it is difficult to align successive masks during the fabrication process. The tolerances of conventional technology thus set a lower limit on the size of the transistor structure, which thereby places a limit on certain of the transistor operating parameters, such as its high frequency limit.

According to one aspect of the present invention there is provided a process for manufacturing an electronic device including a photolithographic masking and chemical etching step in which the photoresist material deposited on the substrate is exposed to light transmitted through the substrate prior to chemical etching.

In more detail, according to the invention, a process for manufacturing an electronic device on a semiconducting substrate which is transparent to light of a particular wavelength includes the steps of:
treating the substrate to form at least one region having a different electrical property to the substrate; and
defining a conducting contact for the region by selective photolithographic masking and chemical etching, including subjecting a layer of photoresist material deposited on one side of the substrate to light of the particular wavelength transmitted through the substrate from a light source on the other side of the substrate.

In one embodiment according to the invention, a process for manufacturing a field effect transistor includes the steps of:
providing a diamond substrate which is transparent to light of a predetermined wavelength;
defining source, gate and drain regions of the transistor on or in the substrate; and
defining contacts for the source, gate and drain regions by selective photolithographic masking and chemical etching, at least one masking and etching step comprising subjecting a layer of photoresist material deposited on one side of the substrate to light of the predetermined wavelength which is passed through the substrate from a light source on the other side of the substrate.

In a further preferred, embodiment, the process includes the steps of:
providing a p-type diamond substrate which is transparent to ultraviolet light;
depositing a layer of insulating material on the surface of the substrate;
depositing a layer of a first metal over the layer of insulating material;
selectively removing the deposited layers to define a gate region of the transistor; forming source and drain regions of the transistor adjacent to the gate area by ion implantation or chemical etching;
depositing a layer of photoresist material over the source, gate and drain regions;
exposing the layer of photoresist material to ultraviolet light which is passed through the substrate;
removing the exposed photoresist material, so that a layer of photoresist material remains above the gate region;
depositing a layer of a second metal over the source, gate and drain regions; and
selectively removing the layer of photoresist material and hence the layer of the second metal above the gate region, a MISFET structure thereby being obtained which has source and drain contacts of the second metal and a gate contact of the first metal.

The layer of insulating materials may comprise an oxide, nitride, oxynitride or carbide.

The first metal is preferably a low work function metal such as aluminium or chrome.

The second metal is preferably a high work function metal such as gold, platinum, gold/tantalum alloy, or palladium.

Figures 1e to 1h illustrate a process for manufacturing a field effect transistor according to the invention, step by step.

In figure 1a, a substrate 10 of p-type diamond material is provided, which is optically transparent. A thin layer 12 of insulating material is deposited on the surface of the substrate 10. The insulating layer 12 comprises an oxide nitride oxynitride or carbide material.

As shown in Figure 1b, a layer 14 of a first metal is deposited over the layer 12 of insulating material. The first metal is a low work function metal, such as aluminium or chrome.

The next step, illustrated by figure 1c, is to define the gate region of the transistor. This is achieved by a conventional photolithographic masking and chemical etching process, which selectively removes the layers 12 and 14, except in the region of the gate (G).

In the next step of the process, source (S) and drain (D) regions are defined in the upper surface of

the substrate 10 by means of ion implantation or by chemical etching of demarcated regions adjacent the gate region. In the case of ion implantation, boron, gallium, carbon or lithium ions can be used. Alternatively, argon etching can be used. The source and drain regions extend into the surface of the substrate 10 as illustrated schematically in Figure 1d.

Referring now to Figure 1e, a layer 16 of photo-resist material which sensitive to ultraviolet (UV) light is deposited over the structure illustrated in Figure 1d. The structure is then subjected to ultra-violet light from beneath the substrate 10. Because the substrate 10 is transparent to ultra-violet light, the photo-resist layer 16 is exposed to this light, except above the gate region (G), where the metallic layer 14 shields the photo-resist layer from the UV light.

The photo-resist layer 16 is subsequently treated with a solvent, which dissolves the layer 16 in the regions where it was exposed to UV light. Thus, following this step, the photo-resist layer 16 is removed, except from the metal layer 14 above the gate region (G). This is illustrated in Figure 1f.

Referring now to Figure 1g, a layer 18 of a second metal is deposited over the entire structure. The second metal is a high work function metal such as gold, platinum, gold/tantalum alloy or palladium.

Finally, as shown in Figure 1h, a lift-of etch technique is used to remove the layer 16 of photo-resist material over the gate region, exposing the metal layer 14. The layer 18 of the second metal is trimmed, removing those portions of the layer which do not lie above the source and drain regions of the transistor. Thus, a MISFET structure is created, with source and drain contacts of the second metal, and a gate contact of the first metal.

Because of the self-aligning effect of exposing the photo-resist layer 16 through the transparent substrate 10, great accuracy is achieved in defining the source, gate and drain contacts relative to one another. In particular, the problem of accurately aligning successive masks during the transistor manufacturing process is avoided.

Claims

1. A process for manufacturing an electronic device characerised in that it includes a photolithographic masking and chemical etching step in which photoresist material (16) deposited on one side of a transparent substrate (10) is exposed to light transmitted through the substrate prior to chemical etching.

2. A process for manufacturing an electronic device on a semiconducting substrate (10) which is transparent to light of a particular wavelength characterised in that it includes the steps of:
treating the substrate (10) to form at least one region (5,D) having a different electrical property to the substrate; and
defining a conducting contact (18) for the region by selective photolithographic masking and chemical etching including subjecting a layer of photoresist material (16) deposited on one sidce of the substrate to light of the particular wavelength transmitted through the substrate from a light source on the other side of the substrate.

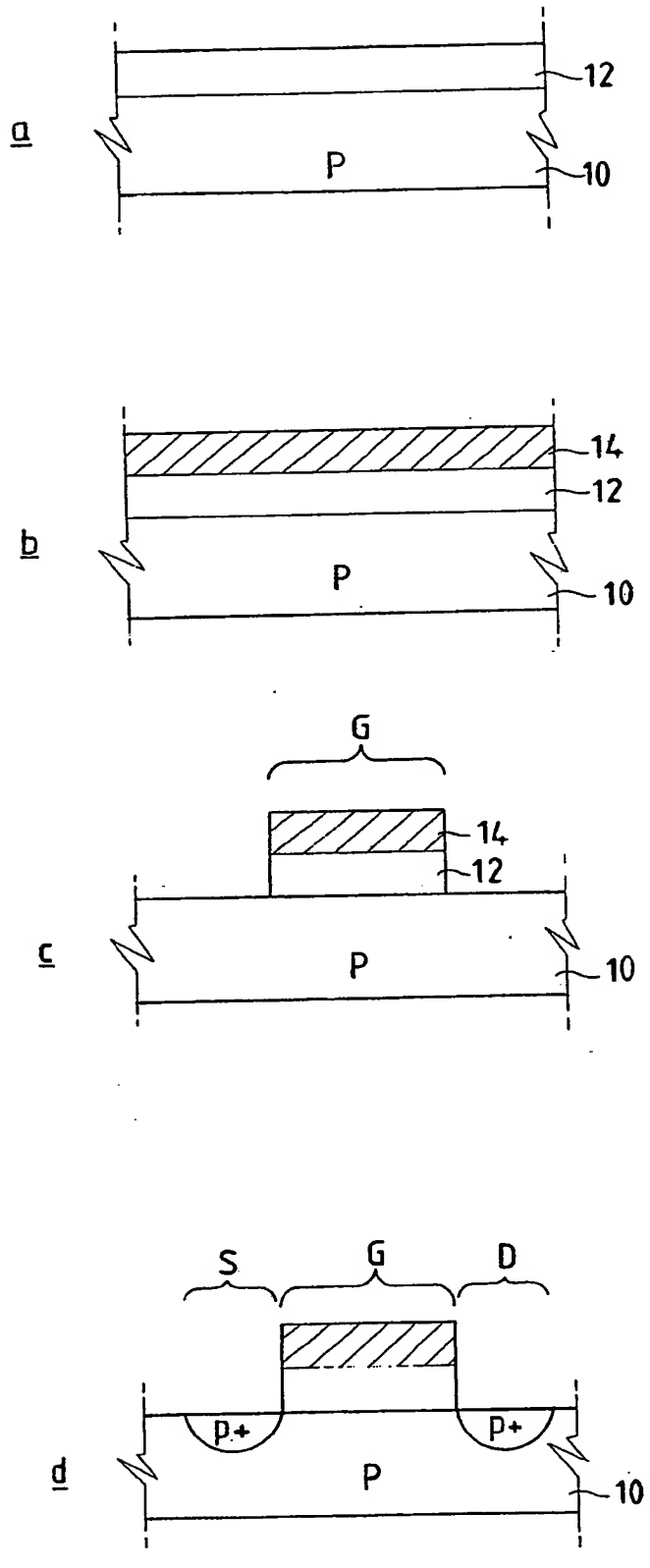
3. A process for manufacturing a field effect transistor characterised in that it includes the step of:
providing a diamond substrate (10) which is transparent to light of a predetermined wavelength:
defining source, gate and drain regions (S,G,D) of the transistor on or in the substrate; and
exposing the layer of photoresist material to ultraviolet light which is passed through the substrate;
removing the exposed photoresist material, so that a layer of photoresist mateial remains above the gate region;
depositing a layer (18) of a second metal over the source, gate and drain regions; and
selectively removing the layer of photoresist material and hence the layer of the second metal above the gate region, a MISFET structure thereby being obtained which has source and drain contacts (5,D) of the second metal (18) and a gate contact (6) of the first metal (14).

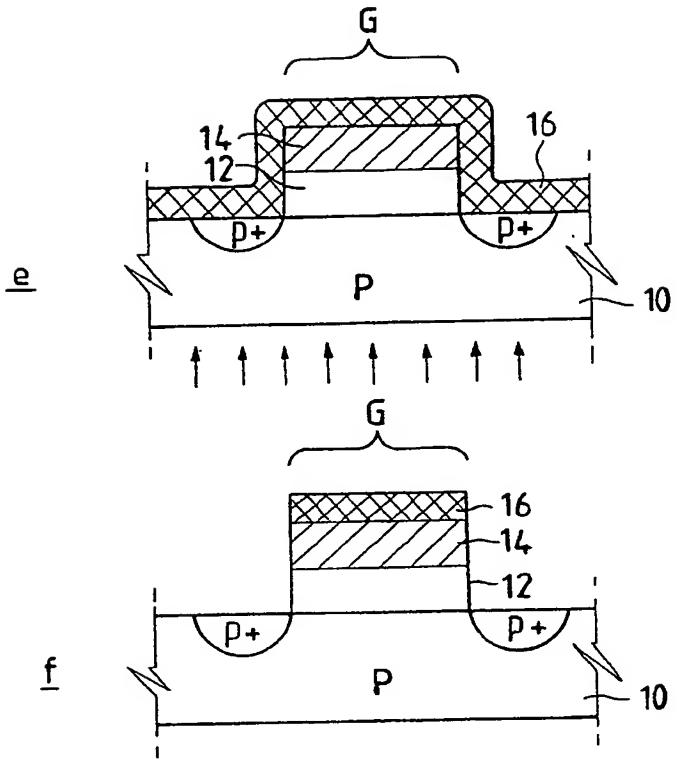
5. A process according to claim 4 characterised in that the layer (12) of insulating material comprises an oxide nitride, oxynitride or carbide.

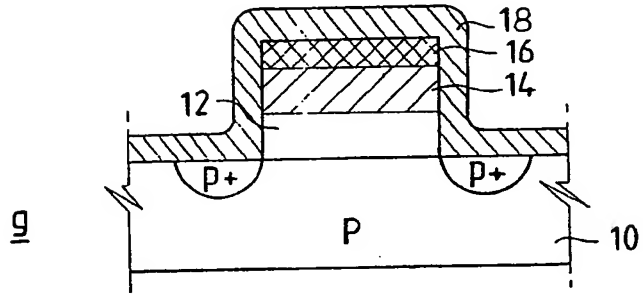
6. A process according to claim 4 or claim 5 characterised in that the first metal (14) is a low work function metal such as aluminium or chrome.

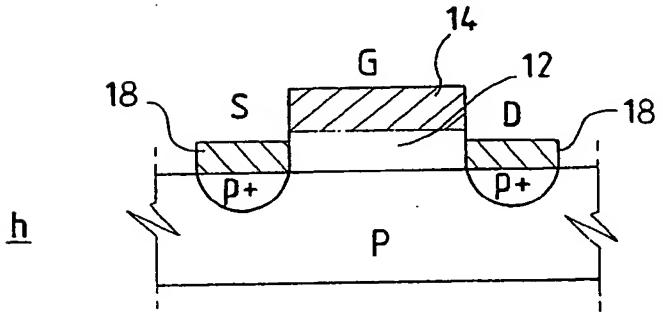
7. A process according to any one of claims 4 to 6 characterised in that the second metal (18) is a high work function metal such as gold, platinum, gold/tantalum alloy, or palladium.

Fig 1









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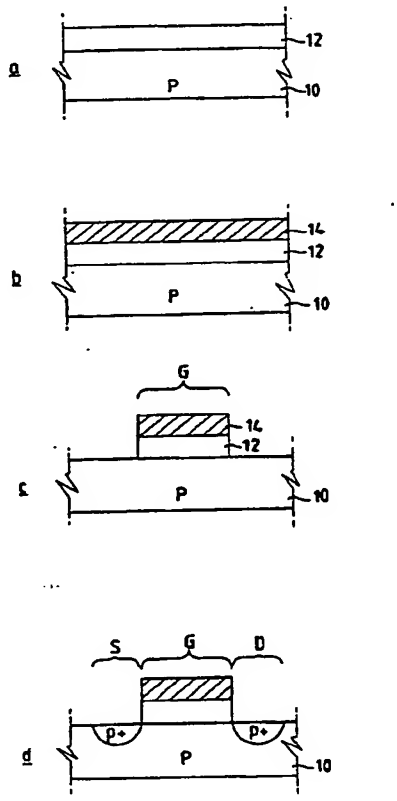

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PARTIAL EUROPEAN SEARCH REPORT

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

Application number
EP 89 30 5258

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	FR-A-2 280 979 (RCA CORP.) * Claims; page 6, line 18 - page 7, line 22; figures * --	1	H 01 L 21/336 H 01 L 29/16 H 01 L 29/784
X	EP-A-0 090 661 (FUJITSU) * Claims; figures * --	1	
A	SOLID STATE TECHNOLOGY, vol. 22, no. 2, February 1979, pages 57-60 R.L. MADDOX: "Advances in double sided wafer processing" * Whole document * ------	1,2	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L

INCOMPLETE SEARCH

The Search Division considers that the present European patent application does not comply with the provisions of the European Patent Convention to such an extent that it is not possible to carry out a meaningful search into the state of the art on the basis of some of the claims.

Claims searched completely: 1,2

Claims searched incompletely:

Claims not searched: 3-7

Reason for the limitation of the search:

Page 9 (claims 3 and 4) is missing

Place of search	Date of completion of the search	Examiner
The Hague	04-05-1990	GELEBART

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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E : earlier patent document, but published on, or after the filing date
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